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Design Low Power Quaternary Adder Using Multi-Value Logic

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ABSTRACT:
This paper presents design of quaternary adder based on multi valued logic. Adders are one of the important part of the processing element and hence it has a focus of research. Therefore implementation of adders using multi valued logic can prove to be very useful. The proposed Quaternary adders are designed with the help of Cmos transistor logic. These Quaternary adders are verified by simulation and appear to have very low power dissipation. Design of the binary logic circuits is limited by the requirement of the interconnections. A possible solution could be arrived at by using a larger set of signals over the same chip area. Multiple-valued logic (MVL) designs are gaining importance from that perspective. This paper presents two types of multiple-valued Quaternary adder circuits, implemented in Multiple-Valued voltage-Mode Logic (MV-VML). First type is designed using Quaternary input to Binary output. Second type is designed by converting the Binary logic to Quaternary code, which enables to implement circuit with reduced hard ware. From these two circuit we implementing Mod-4 Adder circuit. The design is targeted for the 0.18 nm CMOS technology and verification of the design is done on tanner Tools. Area of the designed circuits is less than the corresponding binary circuits and quaternary adders because number of transistors used are less.

INDEX TERMS— *Multi-valued logic, Quaternary adder, adder, CMOS logic, DLC, Mod-4 Adder.*

I. INTRODUCTION

Multi-valued logic is very brilliantly defined by "Elean Dubrova" as like painting a picture having all probable colors available. Multi-value logic is defined as a non-binary logic and involves the switching between more than two states.

Multi-valued logic means instead of assuming one of the two states as per in binary logic, signal may assume one of more than two states, for instant 4 states. Binary values take only values {0,1}.Multi-valued synthesis take multi-valued variables Xi can take values Pi={0,…pi-1}.Multi-valued logic offers vital advantage like more information can be processed over a given set of lines to decrease the burden of interconnections and thereby switching.

The advantage of Multi-valued logic are the use of fewer operations potentially fewer gates and reduction in number of interconnections and switching. The reduction of dynamic power dissipation is VLSI applications is the major challenge for today's engineers as major part of the power is consumed by interconnect and switching. Adders form the basic part of processing element. Adders are basically a circuit which is used in variety of applications. So, if we create an optimized adder simultaneously the processing elements will be improved. This will fasten the calculation of arithmetic Logic Unit which further improves and fasten the performance of the unit. Using an optimized adder using Multi-Valued logic will lessen the space required. Optimized adders will prove to be useful in other Digital Signal Processing as adders are the basic part of Digital Signal Processing. Basic feature of multi-valued logic over binary logic is multi-valued logic requires fewer interconnections, more information can be processed over a given sets of lines, area is reduced, gives faster results, low power dissipation and low cross talk noise.

Current digital electronics technologies are mainly based upon binary systems. Multi-valued systems are usually proposed to provide advantages by decreasing the number of data interconnect lines and processing elements. Such logic circuits can represent numbers with fewer bits than binary, e.g. the decimal number 255 is represented as 1111 1111 in binary and 3333 in quaternary. As the circuits become less complicated, the data processing may be fast and reliable. However, multi-valued logic designs may be challenging due to difficulties in implementation. The idea of the multiple-valued logic, or fuzzy logic opened a vast research area. In 1920, Jan Lukasiewicz begins to create a system of many-valued logic. Later Jan Lukasiewicz and Alfred Tarski together formulated logic on n truth values where n was equal to or more than two. In 1973, Lotifi A Zadeh proposed his theory of fuzzy logic.

Power reduction has been a research goal for several years and there have been many important results achieved. The reduction of system noise, however, is still a lower research priority at the architectural level. Power dissipation in most integrated systems is mainly dynamic and dependent upon the voltage swing magnitude and frequency across load capacitances. Two types of adders are demonstrated in this paper. In the

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first type, Quaternary signals are converted to Binary codes, where as in the second type Binary input is converted to Quaternary code. After addition operation, output is obtained in quaternary, for both the cases Mod-4 Adder is Design. This paper is organized as follows. In section two, Methodology is demonstrated and Explained. In section three, Litarature Review is explained. Section four explains the conclusion part of the paper. In section four Refferance are given

II. METHODOLOGY

Several designing methods have been proposed in the recent papers to realize the Multi-valued logic circuits. They can be fundamentally categorized as current –Mode, voltage mode and mixed mode circuits. Several prototype chips of current-mode CMOS circuits have been fabricated, showing somewhat better performances compared to the corresponding binary circuit. Even though current-mode circuits have been popular and offer several CMOS binary logic circuits from the perspective of dynamic switching activity. Voltage-mode circuits consume a large majority of power only during the logic level switching. Hence, voltage-mode circuits do offer lesser power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity.

Quaternary logic (radix-4-valued) is chosen as the base radix. Using a quaternary radix offers all the benefits of MVL with the important advantage of being able to easily interface with traditional binary logic circuits. Quaternary signals are converted to binary signals before performing arithmetic operations. Results of arithmetic operations are also binary signals. Hence these binary signals are to be converted to quaternary signals. In this paper, quaternary to binary and binary to quaternary converter are designed, and also Modulo-4 arithmetic operations are performed in such a way to get minimum number of gates and minimum depth of net.

A. Principle of operation for Quaternary Coverter Design Circuits.

1) A basic Quaternary to binary converter uses three down literal circuits DLC1, DLC2, DLC3 (each having different threshold voltage) and 2:1 multiplexer .Q is the quaternary input varying as 0, 1, 2 and 3 which is given to three DLC circuits. The binary out puts thus obtained will be in complemented form and are required to pass through inverters to get actual binary numbers. Down literal circuits are realized from basic CMOS inverter by changing the threshold voltages of p-mos and n-mos transistors. Here in this fig. We seen that we use three DLC circuites and output of DLCcircuit is connected to the 2*1 mux and we get the output in the form of binary values. If we gives quaternary inputs output will be binary using mux circuits.

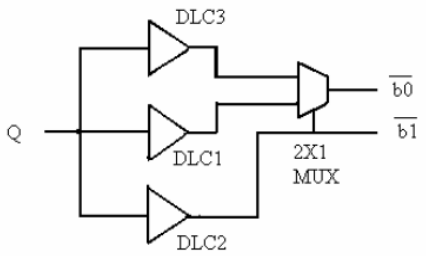

Fig. 1 Quaternary to binary Converter

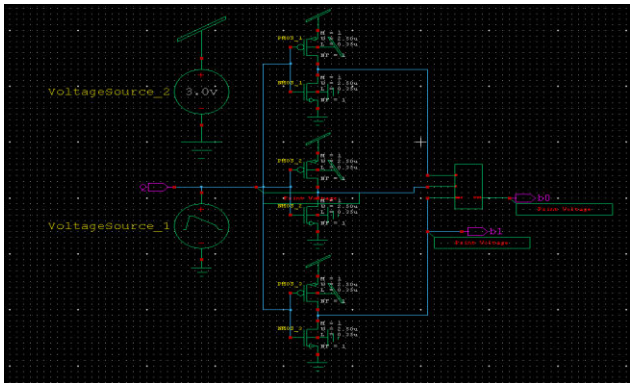

Fig. Schematic of quaternary and Binary Converter

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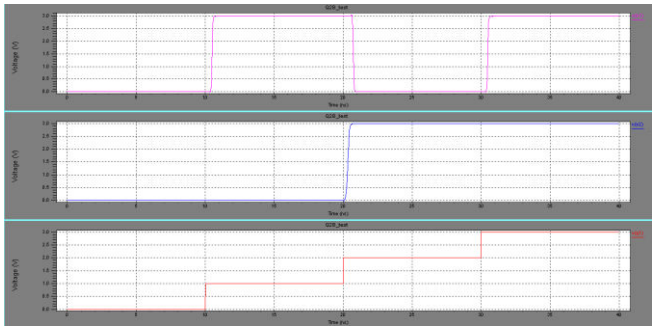

FIG. SIMULATED RESULT OF Q TO B CONVERTER

2) Binary to quaternary converter circuit is shown in the circuit. LSB and MSB of a two bit binary number are given to DLC 1.

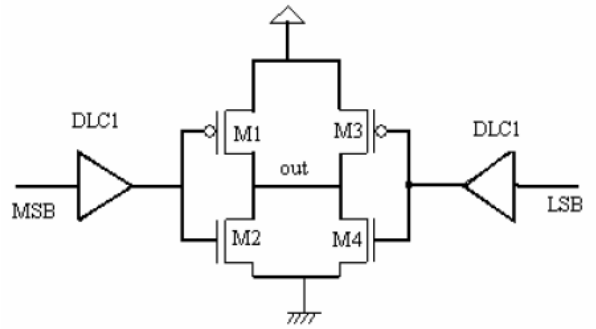

Fig. 2 Block Diagram of Full Adder

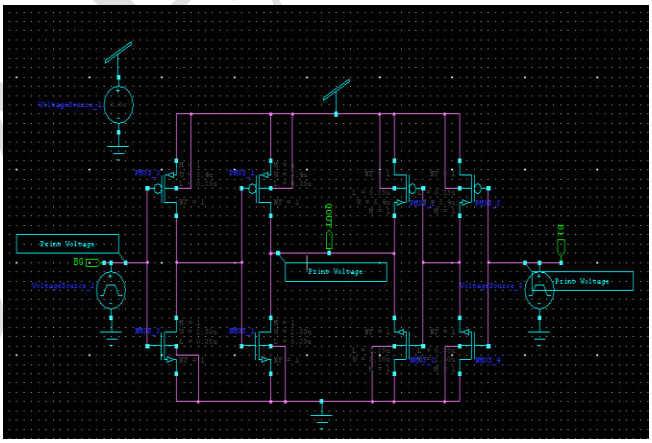

Fig. Schematic of Binary to Quaternary Converter

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Fig. Simulated Result of B to Q Converter

B. Principle of operation for Mod-4 Adder Design Circuits.

Modulo-4 addition: Modulo-4 addition is performed after quaternary to binary conversion. Quaternary inputs 0, 1, 2, 3 are represented in binary as 00, 01, 10, and 11 respectively .

Natural representation of quaternary numbers is shown in table Minimal functions have been obtained from the Karnaugh diagrams for the addition as shown in Table 2. Then simplified as much as possible using all possible gate types. Minimal functions obtained from the minimal polynomials extracted from the Karnaugh diagrams are shown below. Let x1 x2 and y1 y2 be the binary representation of quaternary numbers which has to be added**.**

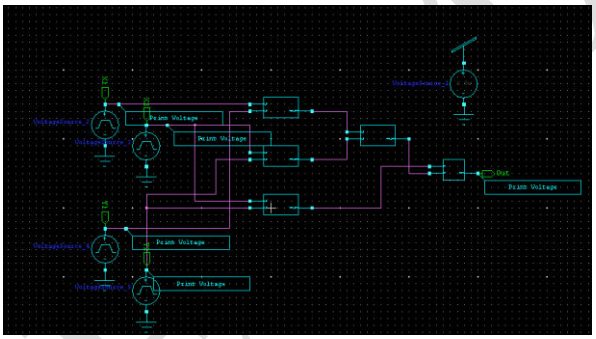

Fig. Proposed modulo-4 adder schematic

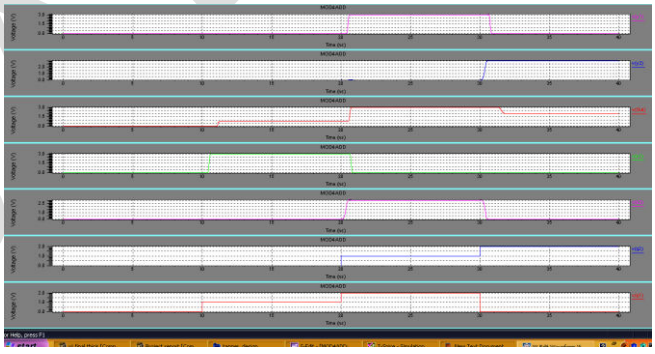

Fig. Simulated Result of Mod-4 Adder.

C. Application Using Max and Min Voltage Logic

Implementing a voltage mode multiple-valued(MV) maximum and minimum function. The circuit has been implemented using Recharge semifloting gates(SFG) transistor. The benefits with this design is,the proposed circuit can easily be fabricated using convetional cmos process. we present a new proposal for implementing a voltage-mode Multiple-Valued (MV) maximum or minimum function. The circuit has been implemented using Recharged Semi Floating-Gate (SFG) transistors. The benefit with this design is, the proposed circuits can easily be fabricated using a conventional CMOS process. The circuit is suitable for a low power design, Vdd < 2 volt. It has high noise margin and good linearity.

The MAX and MIN functions are also fundamental functions in Multiple-valued logic. The MAX function corresponds to the binary function OR, and the MIN function is the AND function in the binary world. The MAX and MIN function has been presented earlier using Neuron- MOS Transistors. However another way of realizing these functions is by using Semi-Floating Gate Recharge Logic. This makes it possible to implement a lowpower digital system with reduced dynamic power dissipation. The advantage of this technology is presented in and the circuit is presented . As we can see the circuit use the analog inverter and the DLC to make a voltage comparator. It then gives a selection signals to the Pass- Gate network, which consists of a pPass-Gate and a nPass- Gate circuit, If the output signal labeled DLC is "high", input1 is selected, and if the signal labeled DLC is "low", input2 is selected. Just by changing the pPass-Gate(nPG) with a nPass-Gate(nPG) and nPG with pPG we can achieve the minimum function as shown in output of the MIN circuit (labeled Minimum) is shown . The heart of this circuit is the analog inverter and the DLC. We know that the analog inverter can be made with high linearity and good precision, just by adjustment of C1 and C2. This is described in . As mentioned in the DLC divides logic levels in the multi-valued logic into a binary state at an arbitrary threshold. The DLC is a 2 input inverter, and by making C4 slightly less than C3, we make sure the threshold voltage is set correct, and the output of the DLC is set "high" when Input1 is equal to Input2, hence PassGate network will work properly[13].

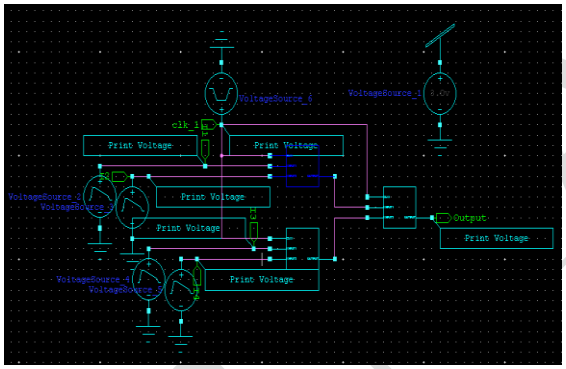

Fig. Schematic Circuit for Min and Max Voltage logic

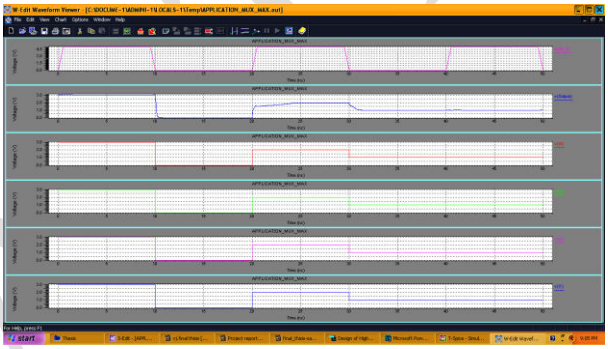

Fig. Simulated Result of min and max voltage logic

III. LITERATURE REVIEW

An exhaustive literature review has been carried out related to the titled work to find out the current research. Abstracts of some of the most relevant research works are reported in the following paragraph

A. Design of Low Power Quaternary Adders in Voltage Mode Multi-Valued Logic Neha Umredkar , Dr. Prof. M. A. Gaikwad, Prof. D. R. Dandekar Volume 3, Issue 1 (Sep. – Oct. 2013) IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3, Issue 1 (Sep. – Oct. 2013), PP 15-21.

Authors have proposed low power quaternary adder using transmission gate [1]. Using this quaternary half adder we have constructed quaternary full adder. The quaternary system is capable of transmitting more information than the binary systems. Low power dissipation is the major advantage offered by the proposed adder. The simulation results are verified at frequency up to 50 Mhz, input supply voltage of maximum 3 Volts. The average power dissipation obtained is 0.023 micro watts for half adder and 0.832 micro watt for full adder. These circuits have been verified for high frequency with low voltage. As adders form the basic computing element, design of quaternary adders using multi valued logic has several advantages in the particular area like communication, memory and digital signal processing.

B. Design of high performance Quaternary adders, Vasundara Patel K, K S Gurumurthy, april 2011 2011 41st IEEE International Symposium on Multiple-Valued Logic.

Authors have proposed high performance quaternary adder using cmos logic and demonstrated a design technique for two types of quaternary full adders [2]. Quaternary full adder (Type I) is designed with down literal circuit, code generators, Sum and Carry blocks. This circuit requires 148 transistors and dissipates 84?W at 250MHz. In Type II full adder, unique encoding for the quaternary input has reduced the requirement of the complex hardware which enables to implement high performance quaternary full adder. This circuit requires 113 transistors and dissipates 91.25 ?W. Simulation of the proposed circuits is carried out targeted for 180nm technology using Synopsis HSPICE and COSMOS tools. These circuits consume less number of transistors and shows high performance compare to the other circuits.

C. Performance of a Quaternary Logic Design Mahsa Dornajafi , Steve E. Watkins, Benjamin Cooper 978-1-4244-2077-3/08/$25.00 ©2008 IEEE.

Authors have proposed and demonstrate quaternary circuit was proposed and a functional simulation of its components has been performed [3]. It was observed that driver circuitry can be used to represent the quaternary logic of the input. One case worked properly, but additional cases had isolated errors. The sensitivity of the performance to the voltage levels will require more analysis. The circuitry of the matrix can be used as a quaternary difference calculator. The circuit receives two inputs and presents the difference between the inputs in four-level logic. The propagation delay of the driver and matrix was analyzed. A typical delay of 8 ns is needed for the circuit to respond to the changes of the input and act in a steady-state situation. The calculated power consumption of the driver was 1.675 mW in the steady-state situation.

B. H. Gundersen And Y. Berg Presented In His Paper "Max And Min Functions Using Multiple-Valued Recharged Semi-Floating Gate Circuits".

In this paper we present a new proposal for implementing a voltage-mode Multiple-Valued (MV) maximum or minimum function. The circuit has been implemented using Recharged Semi Floating-Gate (SFG) transistors. The benefit with this design is, the proposed circuits can easily be fabricated using a conventional CMOS process. The circuit is suitable for a low power design, Vdd < 2 volt. It has high noise margin and good linearity. The simulation results for the proposed circuit are evaluated using AMS 0.35µ*m* CMOS device parameters.

D. A Novel Voltage-Mode CMOS Quaternary Logic Design, Ricardo Cunha G. da Silva, Henri Boudinov, and Luigi Carro IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 53, NO. 6, JUNE 2006.

Author has presented the results on the performance of 0.25-μm gate-length AlGaN/GaN HEMTs with varying field plate length [5]. These devices exhibited high current densities of more than 1.4 A/mm and peak extrinsic transconductance of more than 430 mS/mm. DC *I–V* as well as transfer characteristics were essentially independent of the length of the field plate, but there was significant improvement in breakdown voltage as the length of the field plate increased. With increase in field-plate length, degradation in the values of *fT* and *f*max was observed, but there was significant improvement in power densities. Also, at 18 GHz, a CW output power density of 9.1 W/mm with PAE of 23.7% was obtained for device with a field plate length of 1.1 μm, yielding the highest reported power performance of AlGaN/GaN HEMTs at 18 GHz.

E. Design of High-Performance Quaternary Adders Based on Output-Generator Sharing, Hirokatsu Shirahama and Takahiro Hanyu 38th International Symposium on Multiple Valued Logic.

In this paper, authors have proposed quaternary full adders based on output generator sharing [6]. The use of appropriate Input-value conversion makes it possible to reduce the number of output generators, which enables to implement high performance quaternary full adders. As a result, the delay of the proposed current-mode implementation is reduced to 70 percent and the delay and power dissipation of the proposed voltage-mode implementation are reduced to 73 percent and 79 percent, respectively, in comparison with those of a corresponding CMOS implementation. As a future prospect, it is important to compare the performances of proposed quaternary full adders with those of existing quaternary full adders. Moreover, we will discuss the noise immunity of MV circuits and the techniques to compensate for it because the unit voltage swings are relatively small in the proposed implementations.

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IV. CONCLUSIONS

These Adders are one of the important part of the processing element and hence it has a focus of research. Therefore implementation of adders using multi valued logic can prove to be very useful. As adders form the basic computing element, design of quaternary adders using multi valued logic has several advantages in the particular area like communication, memory and digital signal processing. Quaternary input has reduced the requirement of the complex hardware which enables to implement high performance quaternary full adder. These circuits consume less number of transistors and shows high performance compare to the other circuits. This review concludes that quaternary multi valued logic full adder using cmos domino logic. Using this we have constructed quaternary full adder. The quaternary system is capable of transmitting more information than the binary systems. Low power dissipation is the major advantage offered by the proposed adder. The Quatenary Adder is used in this thesis. In this paper we have discussed and demonstrated a design technique for two types of quaternary full adders. quaternary adder (Type I) is designed with down literal circuit, code generators, Sum and Carry blocks. This circuit requires 148 transistors and dissipates 84μW at 250MHz. In Type II full adder, unique encoding for the quaternary input has reduced the requirement of the complex hardware which enables to implement high performance quaternary full adder. This circuit requires 113 transistors and dissipates 91.25 μW. Simulation of the proposed circuits is carried out targeted for 180nm technology using Tanner EDA tools. These circuits consume less number of transistors and shows high performance compare to the other circuits. The MAX and MIN applications show high linearity, and can be fabricated using a conventional CMOS process. And as we can see, it is easy to make a multiple input MAX- or MIN Circuit just by adding the MAX or MIN circuits.

II. REFFERANCE

[1] Neha Umredkar , Dr. Prof. M. A. Gaikwad, Prof. D. R. Dandekar , “Design of Low Power Quaternary Adders in Voltage Mode Multi-Valued Logic “,IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 3, Issue 1 (Sep. – Oct. 2013), PP 15-21.

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[6] Hirokatsu Shirahama and Takahiro Hanyu, “Design of High-Performance Quaternary Adders Based on Output-Generator Sharing”, 38th International Symposium on Multiple Valued Logic.